


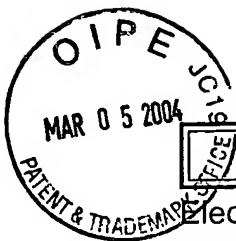


Electronic Filing System (EFS) Data
Electronic Patent Application Submission
USPTO Use Only

EFS ID: 56647
Application ID: 10612849 
Title of Invention: FIFO Memory Devices Having
Multi-Port Cache Memory Arrays
Therein that Support Hidden EDC
Latency and Bus Matching and
Methods of Operating Same
First Named Inventor: Mario Au
Domestic/Foreign Application: Domestic Application
Filing Date: 2003-07-03
Effective Receipt Date: 2004-03-05
Submission Type: Information Disclosure
Statement
Filing Type:
Confirmation number: 6889
Attorney Docket Number: 5646-42DVIP


Total Fees Authorized:

Digital Certificate Holder: cn=Grant J. Scott,ou=Registered Attorneys,ou=Patent and Trademark
Office,ou=Department of Commerce,o=U.S. Government,c=US
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**TRANSMITTAL**

Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention	FIFO Memory Devices Having Multi-Port Cache Memory Arrays Therein that Support Hidden EDC Latency and Bus Matching and Methods of Operating Same									
Application Number: 10/612849 										
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<table border="1"><thead><tr><th>Submitted by:</th><th>Elec. Sign.</th><th>Sign. Capacity</th></tr></thead><tbody><tr><td>Grant J. Scott Registered Number: 36925</td><td>/gjs/</td><td>Attorney</td></tr></tbody></table>			Submitted by:	Elec. Sign.	Sign. Capacity	Grant J. Scott Registered Number: 36925	/gjs/	Attorney		
Submitted by:	Elec. Sign.	Sign. Capacity								
Grant J. Scott Registered Number: 36925	/gjs/	Attorney								
<table><tr><td>Documents being submitted</td><td>Files</td></tr><tr><td>us-ids</td><td>5646-42DVIP-usidst.xml</td></tr><tr><td></td><td>us-ids.dtd</td></tr><tr><td></td><td>us-ids.xsl</td></tr></table>			Documents being submitted	Files	us-ids	5646-42DVIP-usidst.xml		us-ids.dtd		us-ids.xsl
Documents being submitted	Files									
us-ids	5646-42DVIP-usidst.xml									
	us-ids.dtd									
	us-ids.xsl									
Comments										



ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of
Invention

FIFO Memory Devices Having Multi-Port Cache Memory
Arrays Therein that Support Hidden EDC Latency and Bus
Matching and Methods of Operating Same

Application Number: 10/612849



Confirmation Number: 6889

First Named Applicant: Mario Au

Attorney Docket Number: 5646-42DVIP

Art Unit: 2186

Search string: (6557053 or 6366529 or 6259648 or 5442747
or 4888741).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6557053	2003-04-29	Bass et al.	B1	710	29
	2	6366529	2002-04-02	Williams et al.	B1	365	239
	3	6259648	2001-07-10	Kragick	B1	365	230.05
	4	5442747	1995-08-15	Chan et al.		395	164
	5	4888741	1989-12-19	Malinowski		365	230.05

Signature

Examiner Name	Date